REMARKS

This amendment is being filed in response to the Office Action having a mailing date of March 11, 2005. Independent claims 1, 9, 13, 18, and 23 are amended as shown. New claims 28-43 are added. No new matter has been added. With this amendment, claims 1-43 are pending in the application.

In the Office Action, the Examiner indicated that claims 5-8, 10-11, 15-16, 19, 21-22, and 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include the limitations of their base claims, for which the applicant thanks the Examiner. Claims 1-4, 9, 12-14, 17-18, 20, 23-24, and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Feuser (U.S. Patent No. 6,801,956) in view of Poisner (U.S. Patent No. 6,269,443). For the reasons set forth below, the applicant respectfully disagrees with this rejection and requests that all pending claims be allowed.

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

According to one embodiment, a smart card can be automatically reset from a mute mode. A processor on the smart card writes its status to a status register. A device controller checks the status register to determine the status of the processor. If the status information from the status register indicates that the processor has entered the mute mode, the device controller initiates a generation of a reset signal to reset the processor out of the mute mode. *See, e.g.*, the Abstract from the present application.

In one example embodiment, the processor writes its status to the status register via a WRITE line. For example, the processor may regularly write to a bit of the status register to indicate that it is busy, ready, mute, or other status information that indicates the status of the processor and/or the status of related operations and components. The writing to indicate a

transition to the mute mode may be performed in a number of ways. For instance, the processor may write to a bit in the status register to set that bit to some binary value. Alternatively or additionally, an enable line, a disable line, or other technique can be used to allow the processor to provide the status information to the status register or other suitable data storage device. *See, e.g.*, page 11, lines 1-14 and Figures 3-4 of the present application.

In contrast, none of the cited references disclose, teach, or suggest these features. For example, while Feuser does show a status register in Figure 2, there is nothing indicated in Feuser that a processor writes or otherwise stores processor status information into the status register. In fact, a processor is not even shown in Feuser. Column 3, lines 1-9 and 44-47 of Feuser cited by the examiner is completely silent as to processor status information being provided to the status register by the processor. For instance, the status register of Feuser is described as only providing notification about the activity of the interfaces by means of a "USB active" signal, in the case of operation with a USB interface. Clearly, therefore, the information being provided into the status register of Feuser is coming from some external device by way of a USB interface, rather than from a processor of the smart card.

Poisner does not cure the deficiencies of Feuser. Poisner simply discloses a processor failure detection unit that determines if the processor fails to function properly after a reset. As described in further detail on column 3, lines 17-23 of Poisner, the processor failure detection unit 284 determines whether the processor 210 is operating properly by checking to see whether the processor performs a first instruction fetch that addresses a non-volatile memory device 270. The processor failure detection unit 284 may also be implemented with a timer to detect whether the processor 210 is functioning. If the processor 210 fails to reset the timer before the timer expires, a failure is detected. Thus, the failure detection unit 284 of Poisner does not check the status of the processor by looking at the memory device 270 to determine if the processor has stored processor status information therein. Rather, the processor failure detection unit 284 determines whether the processor has failed by determining whether the processor has performed an instruction fetch and/or whether the processor has failed to reset a

timer. Poisner is completely silent as to any feature wherein the processor writes, stores, or otherwise provides processor status information in the non-volatile memory device 270.

Accordingly, claim 1 has been amended to recite that the status information is provided by the processor to the status register. As described above, this is a feature that is not found in any of the cited references. Feuser is completely silent with regards to this feature. Poisner uses different types of techniques to determine processor status, including checking whether the processor has performed an instruction fetch or whether the processor has reset a timer. Accordingly, claim 1 is now in allowable form.

Claim 9 has been amended to recite that the processor status information is provided by a processor to the means for storing processor status information. This is a feature that is not disclosed, taught, or suggested by any of the cited references, and therefore amended claim 9 is now allowable.

Claim 13 is amended to recite receiving from a processor and storing status information associated with a state of the processor. As described above, this feature is missing from Feuser, and Poisner uses different techniques to determine processor status. Poisner does not check stored status information received from a processor. Accordingly, amended claim 13 is now allowable.

Claim 18 is amended to recite instructions to store status information received from a processor. Because this feature is not disclosed, taught, or suggested by any of the cited references, amended claim 18 is now allowable.

Claim 23 is amended to recite a status register coupled to the processor to store status information that is provided by the processor to the status register. This is a feature that is distinctive over the cited references, and therefore, amended claim 23 is now allowable.

New independent claim 28 has been written along the lines of former claims 1 and 7 combined. New independent claim 31 has been written along the lines of former claims 9 and 10 combined. New independent claim 33 has been written along the lines of former claims 9 and 11 combined. New independent claim 35 has been written along the lines of former claims 13 and 15 combined. New independent claim 37 has been written along the lines of former claims

13 and 16 combined. New independent claim 39 has been written along the lines of former claims 18 and 19 combined. New independent claim 42 has been written along the lines of former claims 23 and 25 combined. All of these new independent claims and the claims that are dependent thereon are allowable. The requisite fee for the newly added claims is included along with this amendment.

The specification is amended as shown to correct a grammatical error.

On page 9, paragraph 4 of the Office Action, the Examiner indicated a statement of reasons for the indication of allowable subject matter. In the statement of reasons, the Examiner provided a list of features that were indicative of allowable subject matter. The applicant respectfully notes that the language used by the Examiner in the listing of features does not precisely track the language of the claims in all instances. Therefore, the scope of the claims are determined by the terms used therein and are not to be limited by the specific language used by the Examiner in the statement of reasons.

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

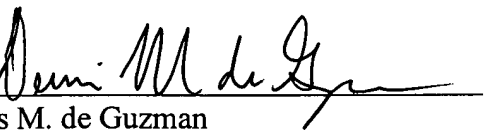
If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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